WF200 数据表：Wi-Fi® 网络协处理器

Silicon Labs WF200 是超低功耗 Wi-Fi® 收发器或网络协处理器 (NCP)，适用于以最佳 RF 性能、低功耗、安全的端到端解决方案以及缩短上市时间作为关键需求的应用。

WF200 集成了平衡-不平衡转换器、T/R 开关、LNA 和 PA，以实现最佳 RF 性能。支持与其他外部 2.4GHz 射频共存。

WF200 针对资源和功率受限的设备在 RF、协议和固件级别进行了优化。节能设备可以在活动模式和睡眠模式下利用这些功能。

对于注重安全的应用，WF200 会提供安全启动功能和安全的加密主机接口。凭借本地集成的真随机数生成器和 OTP 存储器进行保密的加密密钥存储，从而实现可靠的安全性。

WF200 非常适合基于 Linux 和 RTOS 的主机处理器。WF200 支持 802.11 低 MAC 体系结构和 802.11 完整 MAC 体系结构。它通过 SPI 或 SDIO 接口与外部主机控制器通信。

内容要点

- 符合 IEEE 802.11 b/g/n
- TX 功率：+17 dBm（在引脚上）
- RX 灵敏度：-96.7 dBm（在引脚上）
- 支持集成天线分集
- 超低功耗
- 安全且签名的软件
- 加密的主机接口通信
- Linux 和 RTOS 主机支持
- 4x4 QFN32 封装

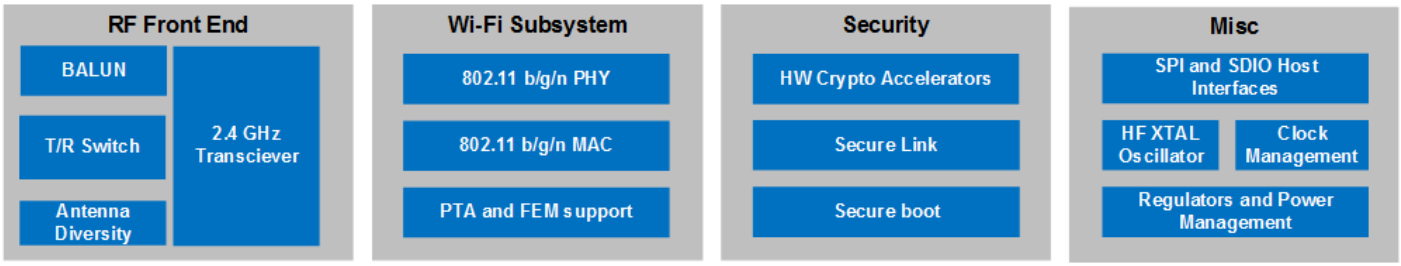


Table of Contents

1. 功能列表

WF200 Wi-Fi 收发器的主要功能如下。

应用
- 工业、家庭和楼宇自动化
- 家用电器
- 安全解决方案
- 零售和商业
- 商业运输
- 消费者医疗
- 运动健身

功能
- 802.11 b/g/n Wi-Fi NCP，包括射频、基带、MAC、安全和主机接口
- 凭借集成的 LNA、PA 和平衡-不平衡转换器实现出色的链路预算
- 包括 OTP，无需外部 EEPROM
- 超低功耗优化解决方案
- 凭借硬件保护的安全加载与加密的主机接口（可选）实现端到端安全性
- 802.11 分割与完整 MAC 体系结构支持
- 完全支持 Linux 和 RTOS 外部主机的网络协处理器 (NCP)

标准/IEEE 802.11 和 WFA
- b - 符号速率：最高 11 Mbps
- g - 符号速率：最高 54 Mbps
- n - 符号速率：最高 72.2Mbps
- d - 监管领域
- e - 遵循 WMM 规范中定义的 QoS
- i - 遵循 WPA2 规范中的定义
- w - 受保护的管理帧
- WMM 省电
- WPA/WPA2 个人/WPA3 个人
- Linux UMAC 支持：
  - WPA2 企业
  - WPS - Wi-Fi 保护设置

主要 MAC 和基带功能
- 1x1 802.11n (20 MHz)，具有完整 802.11 b/g 兼容性，72.2Mbps
- Greenfield Tx/Rx，可实现 802.11n 最佳性能
- 短保护间隔 (SGI)，可实现 802.11n 最佳吞吐量
- A-MPDU Rx 和 Tx，可实现高 MAC 吞吐量
- 多帧的块确认
- Rx 碎片整理
- 支持漫游
- 支持客户端、SoftAP 模式
- 支持不同信道的并发 AP + STA

RF 功能
- Tx 功率：+17 dBm
- Rx 灵敏度：-96.7 dBm
- 2 x 2.4GHz 天线极板，可实现完整的天线分集支持或 FEM 支持
- 2.4GHz 共存；支持 2 线、3 线和 4 线 PTA
- 集成 2.4GHz 的平衡-不平衡转换器、T/R 开关、LNA 和 PA

功耗
- Rx（在 DSSS 为 1Mbps 时）：41.6mA
- Tx（17 dBm，在 DSSS 为 1Mbps 时）：153mA
- 相关 DTIM3 平均电流：298 µA
- 相关睡眠电流：22 µA
- 关机模式：0.5 µA

安全和加密功能
- 安全加载，防回滚
- 加密主机接口，专用硬件加速块
- 集成真随机数生成器
- 使用受保护 OTP 技术的安全密钥存储
- AES/WEP 硬件加速

主机接口
- SDIO（1 位和 4 位 SD 模式，在 26MHz 时）
- SPI（1 位，在 52MHz 时）

外围设备接口
- 外部 32kHz 晶体，用于低功耗
- GPIO（包括唤醒和 Tx/Rx 活动监控）

符合 RoHS/REACH

电气特性
- 1.62V - 3.6V（VDD_D、VDD_{IO}、VDD_{RF}）
- 3.0 - 3.6V (VDD_{PA})

封装
- 4x4 QFN32
- 温度范围：-40°C 至 +105°C

2. Ordering Guide

Table 2.1. WF200 Ordering Information (R Indicates Full Reel)

Part Number	Description
WF200D(R)	WF200 802.11bgn NCP, 4x4 QFN32
WF200SD(R)	WF200 802.11bgn NCP, Secure link interface, 4x4 QFN32

3. System Overview

3.1 Introduction

WF200 is a Wi-Fi network co-processor optimized for RF performance, low energy, and low cost, with two antenna ports, Crystal Oscillator, One Time Programmable Memory, and several GPIOs for interfacing with multi-protocol and RF Front End Module controls.

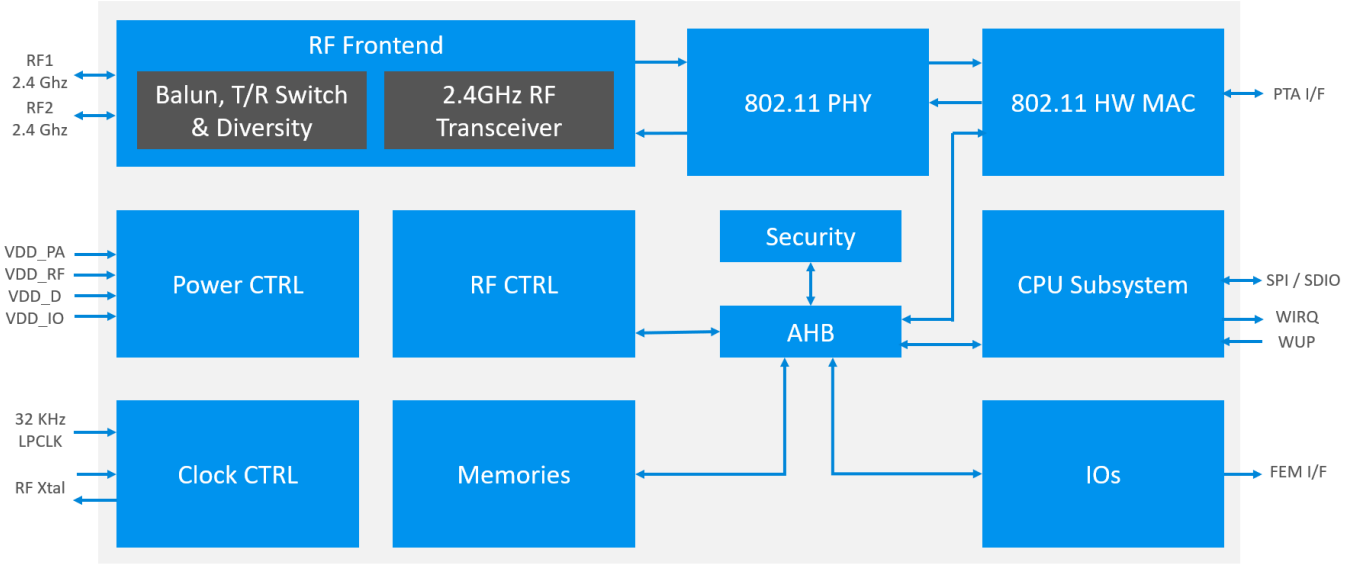


Figure 3.1. WF200 Block Diagram

3.2 Wi-Fi Supported 2.4 GHz Bandwidth and Channels

Supported operating frequencies and bandwidth

Table 3.1. Supported Wi-Fi Modulations, BW, and Channels

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Channel Center Frequency	CHAN	Subject to Regulatory Agency	2412		2484	MHz
Channel Bandwidth	BW		—	20	—	MHz

4. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A = 25 °C; V_{VDD_IO}, V_{VDD_D}, V_{VDD_RF} = 1.8 V; V_{VDD_PA}= 3.3V
- Radio performance numbers are measured in conducted mode, based on Silicon Labs reference designs
- WF200 features and benefits depend on system configuration and may require specific driver, firmware or service activation. Learn more at https://www.silabs.com/products/wireless/wi-fi

Refer to Section 4.2 Operating Conditions for more details about operational supply and temperature limits.

4.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_{STG}		-40	—	150	°C
Junction temperature	TJ_{MAX}		-40	—	125	°C
RF power level at RF1 and RF2 ports	P_{RFMAX}	Max power that can be applied to input of recommended matching network connected to RF1 and RF2 pins.	—	—	10	dBm
Supply voltage to VDD_PA, VDD_RF, VDD_IO, VDD_D	VDD_{MAX}		-0.3	—	3.6	V
Voltage on XTAL_I and XTAL_O pins	VXO_{MAX}		-0.3	—	1.25	V
Voltage on all other pins (GPIO, Host interface, FEM, PTA, etc.)	VG_{MAX}		-0.3	—	VDD_{IO} + 0.3 V	V
Current into any GPIO pin	IO_{MAX}		—	—	20	mA
Sum of current into all GPIO pins	IO_{ALL_MAX}		—	—	150	mA
Range of load impedance at RF1 and RF2 pins during TX	$LOAD_{TX}$		—	—	10:1	VSWR

4.2 Operating Conditions

Table 4.2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient operating temperature	T_A		-40	—	105	°C
Junction operating temperature	T_J		-40	—	125	°C
DC supply voltage to VDD_PA[1]	V_{VDD_PA}		3.0	3.3	3.6	V
Nominal supply voltage to VDD_RF[1]	V_{VDD_RF}		1.62	1.8	3.6	V
Nominal supply voltage to VDD_D	V_{VDD_D}		1.62	1.8	3.6	V
Nominal supply voltage to VDD_IO	V_{VDD_IO}		1.62	1.8	3.6	V

Note:

1. VDD_PA must always be greater than or equal to VDD_RF.

4.3 Power Consumption

Unless otherwise indicated, V_{VDD_PA} = 3.3 V, V_{VDD_D} = V_{VDD_RF} = V_{VDD_IO} = 1.8 V.

Table 4.3. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX mode current	I_{TX}	802.11.b: 1 Mbps, from VDD_PA at 3.3 V	—	108	—	mA
		802.11.b: 11 Mbps, from VDD_PA at 3.3 V	—	104	—	mA
		802.11.g: 6 Mbps, from VDD_PA at 3.3 V	—	101	—	mA
		802.11.g: 54 Mbps, from VDD_PA at 3.3 V	—	95	—	mA
		802.11.n: MCS = 0, from VDD_PA at 3.3 V	—	100	—	mA
		802.11.n: MCS = 7, from VDD_PA at 3.3 V	—	94	—	mA
		802.11.b: 1 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	44.6	—	mA
		802.11.b: 11 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	44.7	—	mA
		802.11.g: 6 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	46.2	—	mA
		802.11.g: 54 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	46.8	—	mA
		802.11.n: MCS = 0, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	46.1	—	mA
		802.11.n: MCS = 7, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	46.8	—	mA
RX mode current	I_{RX}	802.11.b: 1 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	41.6	—	mA
		802.11.b: 11 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	42.3	—	mA
		802.11.g: 6 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	44.7	—	mA
		802.11.g: 54 Mbps, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	47.1	—	mA
		802.11.n: MCS = 0, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	44.5	—	mA
		802.11.n: MCS = 7, from 1.8 V supplies (VDD_RF, VDD_D, VDD_IO)	—	47.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sleep current on power supply pins[1]	I_{SLEEP}	VDD_PA pin, V_{VDD_PA} = 3.3 V	—	66	—	nA
		VDD_RF pin, V_{VDD_RF} = 1.8 V	—	87	—	nA
		VDD_D pin, V_{VDD_D} = 1.8 V	—	18.6	—	µA
		VDD_IO pin, V_{VDD_IO} = 3.3 V	—	3.5	—	µA
Snooze current on power supply pins[2]	I_{SNOOZE}	VDD_PA pin, V_{VDD_PA} = 3.3 V	—	66	—	nA
		VDD_RF pin, V_{VDD_RF} = 1.8 V	—	536	—	µA
		VDD_D pin, V_{VDD_D} = 1.8 V	—	610	—	µA
		VDD_IO pin, V_{VDD_IO} = 3.3 V	—	51	—	µA
Shutdown current on power supply pins[3]	$I_{SHUTDOWN}$	VDD_PA pin, V_{VDD_PA} = 3.3 V	—	67	—	nA
		VDD_RF pin, V_{VDD_RF} = 1.8 V	—	67.4	—	nA
		VDD_D pin, V_{VDD_D} = 1.8 V	—	16.4	—	nA
		VDD_IO pin, V_{VDD_IO} = 3.3 V	—	49	—	nA
Average current for DTIM=1 Interval Profile[4]	I_{LP_DTIM1}	VDD_PA pin, V_{VDD_PA} = 3.3 V	—	154	—	nA
		VDD_RF pin, V_{VDD_RF} = 1.8 V	—	437	—	µA
		VDD_D pin, V_{VDD_D} = 1.8 V	—	454	—	µA
		VDD_IO pin, V_{VDD_IO} = 3.3 V	—	3.7	—	µA
Average current for DTIM=3 Interval Profile[4]	I_{LP_DTIM3}	VDD_PA pin, V_{VDD_PA} = 3.3 V	—	128	—	nA
		VDD_RF pin, V_{VDD_RF} = 1.8 V	—	128	—	µA
		VDD_D pin, V_{VDD_D} = 1.8 V	—	166	—	µA
		VDD_IO pin, V_{VDD_IO} = 3.3 V	—	3.6	—	µA
Average current for DTIM=10 Interval Profile[4]	I_{LP_DTIM10}	VDD_PA pin, V_{VDD_PA} = 3.3 V	—	118	—	nA
		VDD_RF pin, V_{VDD_RF} = 1.8 V	—	38	—	µA
		VDD_D pin, V_{VDD_D} = 1.8 V	—	65	—	µA
		VDD_IO pin, V_{VDD_IO} = 3.3 V	—	3.7	—	µA

Note:

1. All memory is retained in sleep mode. WUP on timer and/or interrupt.
2. All memory is retained and Xtal oscillator is kept on if no 32 kHz clock is provided.
3. Requires complete start-up sequence to resume operation.
4. All DTIM currents assume a 1 ms beacon time duration with a beacon interval of 102.4ms from the AP.

4.4 RF Transmitter General Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, V_{VDD_IO} = V_{VDD_D} = V_{VDD_RF} = 1.8 V; V_{VDD_PA}= 3.3V, center frequency = 2,442 MHz, and measured in 50 Ω test equipment attached at antenna port.

Measurements for this specification are made using the RF_1 port. See Section 5.4.1 Antenna Ports.

4.4.1 RF Transmitter Characteristics

Table 4.4. RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum RMS Output Power at pin[1] [2]	$POUT_{MAX\_RMS\_HPPA\_PIN}$	802.11b: 1 Mbps	—	17.0	—	dBm
		802.11b: 11 Mbps	—	16.0	—	dBm
		802.11g: 6 Mbps	—	15.6	—	dBm
		802.11g: 54 Mbps	—	12.1	—	dBm
		802.11n: MCS=0	—	15.3	—	dBm
		802.11n: MCS=7	—	10.7	—	dBm
Maximum RMS Output Power at Antenna (High Power PA) [2]	$POUT_{MAX\_RMS\_HPPA}$	802.11b: 1 Mbps	—	16.7	—	dBm
		802.11b: 11 Mbps	—	15.6	—	dBm
		802.11g: 6 Mbps	—	15.2	—	dBm
		802.11g: 54 Mbps	—	11.7	—	dBm
		802.11n: MCS=0	—	14.9	—	dBm
		802.11n: MCS=7	—	10.3	—	dBm
Second Harmonic Level for POUT_MAX_PA Setting	$H2_{MAX}$	802.11b: 1 Mbps	—	-48	—	dBm
		802.11b: 11 Mbps	—	-52	—	dBm
		802.11g: 6 Mbps	—	-48	—	dBm
		802.11g: 54 Mbps	—	-50	—	dBm
		802.11n: MCS=0	—	-49	—	dBm
		802.11n: MCS=7	—	-51	—	dBm
Carrier Suppression per 802.11-2012 for POUT_MAX PA setting	C_{SUP}	802.11b: 1 Mbps	—	-50	—	dBr
		802.11b: 11 Mbps	—	-45	—	dBr
		802.11g: 6 Mbps	—	-32	—	dBr
		802.11g: 54 Mbps	—	-42	—	dBr
		802.11n: MCS=0	—	-33	—	dBr
		802.11n: MCS=7	—	-38	—	dBr
POUT variation from VDD_PA=3.0 V to 3.6 V	$POUT_{MAX\_VAR\_V}$	VDD_PA = 3.0 V to 3.6 V, Measured on single channel	—	1.1	—	dB
POUT variation across temperature	$POUT_{MAX\_VAR\_T}$	25C to 85C	—	1.7	—	dB
POUT backoff variation from 50 Ω load specified VSWR[3]	VSWR	up to 2:1 VSWR	—	—	3.0	dB
		up to 3:1 VSWR	—	—	5.0	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. This is the maximum output level at the RF pin with optimum load impedance of 18.6-j9.6 Ω.
2. Rated power levels may not apply to the edge channels, which may need additional backoff for FCC compliance.
3. The maximum backoff levels are for MCS7 and channels 2 to 10. Backoff for channels 1 and 11 to ensure band-edge compliance are detailed in UG382: WF200 Hardware Design User's Guide.

4.5 RF Receiver General Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, V_{VDD_IO} = V_{VDD_D} = V_{VDD_RF} = 1.8 V; V_{VDD_PA}= 3.3V, center frequency = 2,442 MHz, and measured in 50 Ω test equipment attached at antenna port.

Measurements for this specification are made using the RF_1 port. See Section 5.4.1 Antenna Ports.

4.5.1 RF Receiver Characteristics

Table 4.5. RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity for 8% FER (1024 Octet)	$SENS_B$	802.11b: 1 Mbps, at antenna	—	-96.3	—	dBm
		802.11b: 1 Mbps, at pin	—	-96.7	—	dBm
		802.11b: 11 Mbps, at antenna	—	-88.3	—	dBm
		802.11b: 11 Mbps, at pin	—	-88.7	—	dBm
RX Sensitivity for 10% PER (1024 Octet)	$SENS_G$	802.11g: 6 Mbps, at antenna	—	-91.6	—	dBm
		802.11g: 6 Mbps, at pin	—	-92	—	dBm
		802.11g: 54 Mbps, at antenna	—	-74.8	—	dBm
		802.11g: 54 Mbps, at pin	—	-75.2	—	dBm
RX Sensitivity for 10% PER (4096 Octet)	$SENSE_N$	802.11n: MCS=0, at antenna	—	-91.1	—	dBm
		802.11n: MCS=0, at pin	—	-91.5	—	dBm
		802.11n: MCS=7, at antenna	—	-71.8	—	dBm
		802.11n: MCS=7, at pin	—	-72.2	—	dBm
Adjacent Channel (± 30 MHz) Selectivity with desired signal at 6 dB above reference sensitivity for 8% FER (1024 Octet)	ACS_{WB}	802.11b: 1 Mbps	—	54.4	—	dBc
		802.11b: 11 Mbps	—	40.4	—	dBc
Adjacent Channel (± 25 MHz) Selectivity with desired signal at 3 dB above reference sensitivity for 10% PER (1024 Octet)	ACS_{WG}	802.11g: 6 Mbps	—	45.4	—	dBc
		802.11g: 54 Mbps	—	32.9	—	dBc
Adjacent Channel (± 25 MHz) Selectivity with desired signal at 3 dB above reference sensitivity for 10% FER (4096 Octet)	ACS_{WN}	802.11n: MCS=0	—	45.9	—	dBc
		802.11n: MCS=7	—	30.5	—	dBc
2nd Adjacent Channel Selecitivity (± 50 MHz) with desired at 6 dB above reference sensitivity 8% FER (1024 Octet)	$A2CS_{WB}$	802.11b: 1 Mbps	—	59.7	—	dBc
		802.11b: 11 Mbps	—	52.1	—	dBc
2nd Adjacent Channel Selecitivity (± 50 MHz) with desired at 3 dB above reference sensitivity 10% PER (1024 Octet)	$A2CS_{WG}$	802.11g: 6 Mbps	—	55.1	—	dBc
		802.11g: 54 Mbps	—	38.2	—	dBc
2nd Adjacent Channel Selecitivity (± 50 MHz) with desired at 3 dB above reference sensitivity 10% PER (4096Octet)	$A2CS_{WN}$	802.11n: MCS=0	—	54.8	—	dBc
		802.11n: MCS=7	—	35.7	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Max Strong Signal for 8% FER (1024 Octet)	RX_{SAT_B}	802.11b: 1 Mbps	—	-4.0	—	dBm
		802.11b: 11 Mbps	—	-10.0	—	dBm
RX Max Strong Signal for 10% PER (1024 Octet)	RX_{SAT_G}	802.11g: 6 Mbps	—	-9.0	—	dBm
		802.11g: 54 Mbps	—	-9.0	—	dBm
RX Max Strong Signal for 10% PER (4096 Octet)	RX_{SAT_N}	802.11n: MCS=0	—	-9.0	—	dBm
		802.11n: MCS=7	—	-9.0	—	dBm
U/D wtih desired at 6 dB above reference sensitivity for 8% FER (1024 Octet)	$OOBB_B$	802.11b: 1 Mbps : GSM Blocker at 893.8 MHz	—	76.0	—	dB
		802.11b: 1 Mbps : GSM Blocker at 960 MHz	—	75.0	—	dB
		802.11b: 1 Mbps : GSM Blocker at 1879.8 MHz	—	64.0	—	dB
		802.11b: 1 Mbps : GSM Blocker at 1989.8 MHz	—	63.0	—	dB
		802.11b: 1 Mbps : LTE Blocker at 893.8 MHz	—	76.0	—	dB
		802.11b: 1 Mbps : LTE Blocker at 960 MHz	—	75.0	—	dB
		802.11b: 1 Mbps : LTE Blocker at 1879.8 MHz	—	65.0	—	dB
		802.11b: 1 Mbps : LTE Blocker at 2506 MHz	—	56.0	—	dB
U/D with desired at 3 dB above reference sensitivity for 10% PER (1024 Octet)	$OOBB_G$	802.11g: 6 Mbps : GSM Blocker at 893.8 MHz	—	81.0	—	dB
		802.11g: 6 Mbps : GSM Blocker at 960 MHz	—	80.0	—	dB
		802.11g: 6 Mbps : GSM Blocker at 1879.8 MHz	—	69.0	—	dB
		802.11g: 6 Mbps : GSM Blocker at 1989.8 MHz	—	67.0	—	dB
		802.11g: 6 Mbps : LTE Blocker at 893.8 MHz	—	75.0	—	dB
		802.11g: 6 Mbps : LTE Blocker at 960 MHz	—	74.0	—	dB
		802.11g: 6 Mbps : LTE Blocker at 1879.8 MHz	—	62.0	—	dB
		802.11g: 6 Mbps : LTE Blocker at 2506 MHz	—	57.0	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
U/D with desired at 3 dB above reference sensitivity for 10% PER (4096 Octet)	$OOBB_N$	802.11n: MCS=7 : GSM Blocker at 893.8 MHz	—	55.0	—	dB
		802.11n: MCS=7 : GSM Blocker at 960 MHz	—	54.0	—	dB
		802.11n: MCS=7: GSM Blocker at 1879.8 MHz	—	45.0	—	dB
		802.11n: MCS=7: GSM Blocker at 1989.8 MHz	—	44.0	—	dB
		802.11n: MCS=7: LTE Blocker at 893.8 MHz	—	54.0	—	dB
		802.11n: MCS=7 : LTE Blocker at 960 MHz	—	53.0	—	dB
		802.11n: MCS=7 : LTE Blocker at 1879.8 MHz	—	42.0	—	dB
		802.11n: MCS=7 : LTE Blocker at 2506 MHz	—	38.0	—	dB
RX Channel power Indicator Step Size	$RCPI_{STEP}$	802.11b: 1 Mbps	—	0.5	—	dBm
		802.11g: 6 Mbps	—	0.5	—	dBm
		802.11n: MCS=7	—	0.5	—	dBm

4.6 Reference Oscillator and Clock Characteristics

There are two options for the 38.4 MHz Reference Oscillator. Use an external oscillator like a TCXO, or use a crystal with the internal oscillator. The operating temperature range of the application will be limited by the selected component's operating temperature specification. To achieve lowest power operation during power save modes, a 32.768 KHz clock is also required.

4.6.1 Crystal Requirements for using Internal Oscillator

The choice of the crystal affects several parameters including control settings, RF performance, frequency accuracy, and average current consumption in applications that incorporate periodic wake and sleep states. The frequency accuracy of the crystal is the main contributor to Wi-Fi frequency accuracy which must be within +/-25ppm tolerance for 802.11 b, g, and n, in 20MHz channel operation over all of the operating conditions. Refer to UG382: WF200 Hardware Design User's Guide for more details.

Table 4.6. Crystal Requirements for Using Internal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Frequency of HF Crystal Oscillator	$XTAL_{FNOM}$		—	38.4	—	MHz
Frequency tolerance of crystal over all conditions	$XTAL_{FTOL}$		-25	—	25	ppm
Crystal Load Cap	HFX_{CL}		8	10	12	pF
Equivalent Series Resistance	HFX_{ESR}		—	20	40	Ω
Motional Capacitance	HFX_{CM}		2	—	4	fF
Motional Inductance	HFX_{LM}		4	—	8	mH
Shunt Capacitance	HFX_{CS}		—	0.8	2	pF
Pulling Sensitivity	HFX_{PULL}		8	12	20	ppm/pF
Crystal withstanding drive strength	HFX_{DL}		—	—	200	uW
Quality Factor	HFX_{Q}		35000	—	—	
Spurious Mode Series Resistance	HFX_{SPUR}	± 0.7 MHz away from XTAL_FNOM	1100	—	—	Ω
Insulation Resistance 100 V	HFX_{IR}		500	—	—	MΩ

4.6.2 External Oscillator Required Characteristics

An external oscillator, like a TCXO, must provide a stable and high quality signal in order for this IC to meet its performance specifications. This section lists some of the requirements. If the host powers down the TCXO when going into a low power state, the host must also turn on the TCXO in advance of any transceiver activity.

Table 4.7. Reference Oscillator Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal frequency of HF crystal oscillator	$TCXO_{FNOM}$		—	38.4	—	MHz
Frequency tolerance of TCXO over all conditions	$TCXO_{FTOL}$		-20	—	20	ppm
Load Resistance of TCXO	$TCXO_{RL}$		7	10	15	KOhm
Load capacitance of TCXO	$TCXO_{CL}$		6	10	15	pF
Output level of TCXO	$TCXO_{LEVEL}$		0.7	0.9	1.2	V p-p
Symmetry of TCXO	$TCXO_{SYMT}$		45	50	55	%
Startup time of TCXO	$TCXO_{START}$		—	—	2	ms
SSB Phase Noise of TCXO	SSB1	10Hz offset	—	—	-100	dBc/Hz
SSB Phase Noise of TCXO	SSB2	100Hz offset	—	—	-110	dBc/Hz
SSB Phase Noise of TCXO	SSB3	1KHz offset	—	—	-130	dBc/Hz
SSB Phase Noise of TCXO	SSB4	10KHz offset	—	—	-145	dBc/Hz
SSB Phase Noise of TCXO	SSB5	100KHz offset	—	—	-150	dBc/Hz
SSB Phase Noise of TCXO	SSB6	1 MHz offset	—	—	-150	dBc/Hz

4.6.3 Low Power 32.768 kHz Clock Input Requirements

Table 4.8. Low Power 32.768 kHz Clock Input Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Frequency of LP_CLK	$FNOM_{LPCLK}$		—	32.768	—	KHz
Frequency Tolerance of LP_CLK over all conditions[1]	$FTOL_{LPCLK}$		-1000	—	1000	ppm
Load of LP_CLK pin	R_{LPCLK}		—	30	—	KOhm
Input Level at LP_CLK	$SIGL_{LPCLK}$		0.7 * VDD_IO	—	VDD_IO	V p-p
Symmetry of LP_CLK	$DUTY_{LPCLK}$		—	50	—	%

Note:
1. To optimize power consumption in DTIM modes, it is recommended that the frequency drift of LP_CLK within 1 second be lower than +- 100ppm.

4.7 Interface Terminal Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, V_{VDD_IO} = V_{VDD_D} = V_{VDD_RF} = 1.8 V; V_{VDD_PA}= 3.3V, center frequency = 2,442 MHz, and measured by 50 Ω test equipment attached at antenna port.

4.7.1 Supply Terminal Specifications

There are four supply pins to attach to DC power sources: VDD_PA, VDD_RF, VDD_D and VDD_IO.

Please refer to the section on 4.2 Operating Conditions for details on allowed voltages on these pins.

4.7.2 Digital I/O Terminal Specifications

Table 4.9. Digital I/O Terminal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage input low (relative to V_{VDD_IO})	V_{IL}		—	—	30	%
Voltage input high (relative to V_{VDD_IO})	V_{IH}		70	—	—	%
Logic low output voltage (relative to V_{VDD_IO})	V_{OL}	Sinking 5 mA, V_{VDD_IO} ≥ 1.62 V	—	—	25	%
Logic high output voltage (relative to V_{VDD_IO})	V_{OH}	Sourcing 5 mA, V_{VDD_IO} ≥ 1.62 V	80	—	—	%
Input leakage current	I_{Leak}		—	1	—	nA
Pullup resistance	R_{PU}		30	43	65	kΩ
Pulldown resistance[1]	R_{PD}		30	43	65	kΩ
Output fall time from V_{OH} to V_{OL}	T_{OF}	50 pF load, V_{VDD_IO} = 1.62 V	—	15	—	ns
Output rise time from V_{OL} to V_{OH}	T_{OR}	50 pF load, V_{VDD_IO} = 1.62 V	—	15	—	ns

Note:
1. RESETn pin has only pull-up resistance.

4.8 Host Interface

The host interface allows control of WF200 by an MCU or SoC using either SPI or SDIO. Selection between SPI and SDIO is done upon the logic state on SDIO_DAT2/HIF_SEL pin during the rising edge of RESETn signal. If this signal is HIGH, the host interface is configured as SDIO, otherwise it is configured as SPI. The tables below summarizes the pin configurations for the two modes and the achievable speeds on both interfaces

Table 4.10. WF200 SPI and SDIO interface pin configuration

WF200 Pin Name	SPI Mode		SDIO Mode	
RESETn	0 -> 1	1	0 -> 1	1
SDIO_DAT2/HIF_SEL	0	x	1	SDIO_DAT2
SDIO_CLK/SPI_CLK	x	SPI_CLK	x	SDIO_CLK
SDIO_CMD/SPI_MOSI	x	SPI_MOSI	x	SDIO_CMD

WF200 Pin Name	SPI Mode		SDIO Mode	
SDIO_DAT0/SPI_MISO	x	SPI_MISO	x	SDIO_DAT0
SDIO_DAT1/SPI_WIRQ	x	WIRQ (interrupt request to the SPI host)	x	SDIO_DAT1
SDIO_DAT3/SPI_CSn	x	SPI_CSn	x	SDIO_DAT3

Table 4.11. Host Interface Speeds

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO V2.0 clock rate	SD_{Rate}	Host Interface SDIO DS Mode	—	—	26	MHz
		Host Interface SDIO HS Mode	—	—	52	MHz
SPI clock rate	SPI_{Rate}	Host Interface SPI	—	—	52	MHz

Besides the main host interface signals, a couple of other pins also complement the host interface. See AN1219 for more details:

- The GPIO/WUP pin should be used by the host to wake up the WF200 when in power-save mode. This pin is programmable and if power save is not enabled on the device, this pin can be configured as a GPIO. Note that this pin should be LOW to enable the WF200 to reach sleep or shutdown modes.
- GPIO/WIRQ can also optionally be used as a duplication of the IRQ signal from SPI or SDIO. If this is not required, the pin can be configured as a GPIO.

4.8.1 SPI Specification

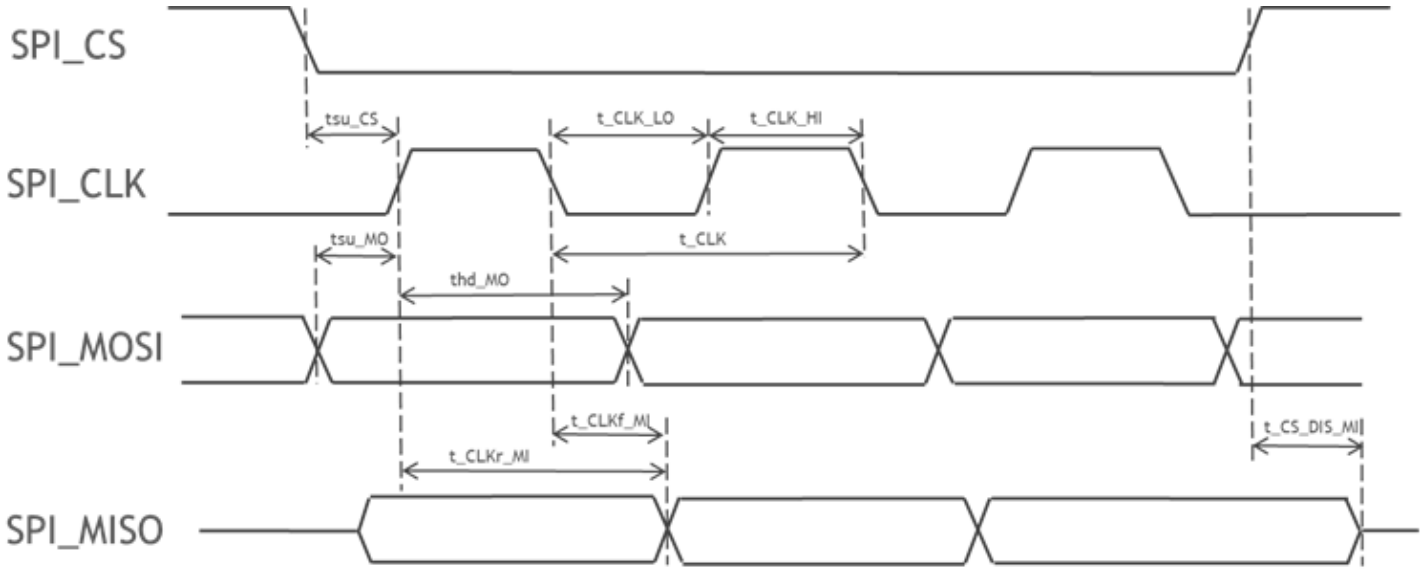


Figure 4.1. SPI Interface Timing Parameters

Table 4.12. SPI Interface Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	19.23[1]			ns
t_{CLK_HI}	Clock high	9			ns
t_{CLK_LO}	Clock low	9			ns
$t_{CS\_DIS\_MI}$	CS disable to MISO. VDD_{IO} = 3.3V			8	ns
	CS disable to MISO. VDD_{IO} = 1.8V			10	ns
t_{SU_CS}	CS setup time	3			ns
t_{SU_MO}	MOSI setup time	3			ns
t_{HD_MO}	MOSI hold time	3			ns
t_{CLKr_MI}, t_{CLKf_MI}	CLK to MISO out; VDD_{IO} = 3.3V			10	ns
	CLK to MISO out; VDD_{IO} = 1.8V			21	ns

Note:

1. 19.23 ns = 1/52 MHz
2. MISO can optionally be latched either on rising edge or falling edge of CLK
3. All timing parameters valid for output load up to 2 mA

4.8.2 SDIO Specification

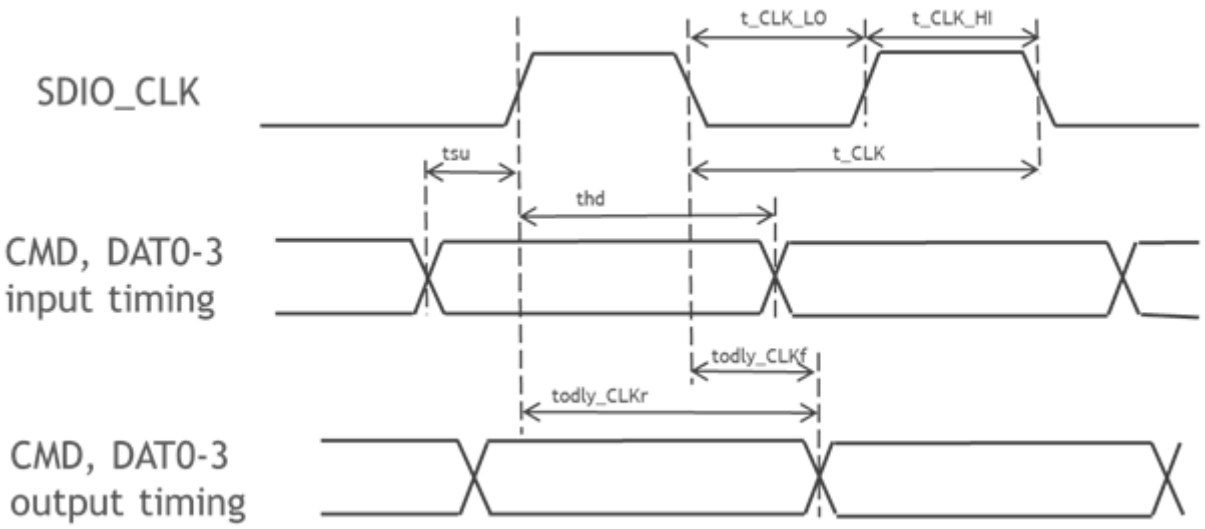


Figure 4.2. SDIO Interface Timing Parameters

Table 4.13. SDIO Interface Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Conditions
t_{CLK_HS}	Clock period in high speed mode	19.23			ns	CL ≤ 20pF
t_{CLK_DS}	Clock period in default speed mode	38.46			ns	CL ≤ 20pF
t_{CLK_LO}	Clock low time	9			ns	CL≤ 20pF
t_{CLK_HI}	Clock high time	9			ns	CL≤ 20pF
CMD, DAT0~3 Inputs (with reference to SDIO_CLK)						
t_{SU}	Input Set time	3			ns	CL≤ 20pF
t_{HD}	Input Hold time	3			ns	CL≤ 20pF
CMD, DAT0~3 Outputs (with reference to SDIO_CLK)						
t_{ODLY_CLKr}, t_{ODLY_CLKf}	Output delay time (relative to rising and falling edge) for VDD = 3.3V			11	ns	VDD_{IO} = 3.3V; CL≤ 20pF
	Output delay time (relative to rising and falling edge) for VDD = 1.8V			22	ns	VDD_{IO} = 1.8V; CL≤ 20pF
t_{OH}	Output Hold time	3			ns	CL≤ 20pF

1. Output data can be latched either on rising edge (HS mode) or falling edge (DS mode) of CLK
2. All timing parameters valid for output load of up to 2 mA

5. Typical Applications and Connections

5.1 Typical Application Circuit for SDIO Host Interface

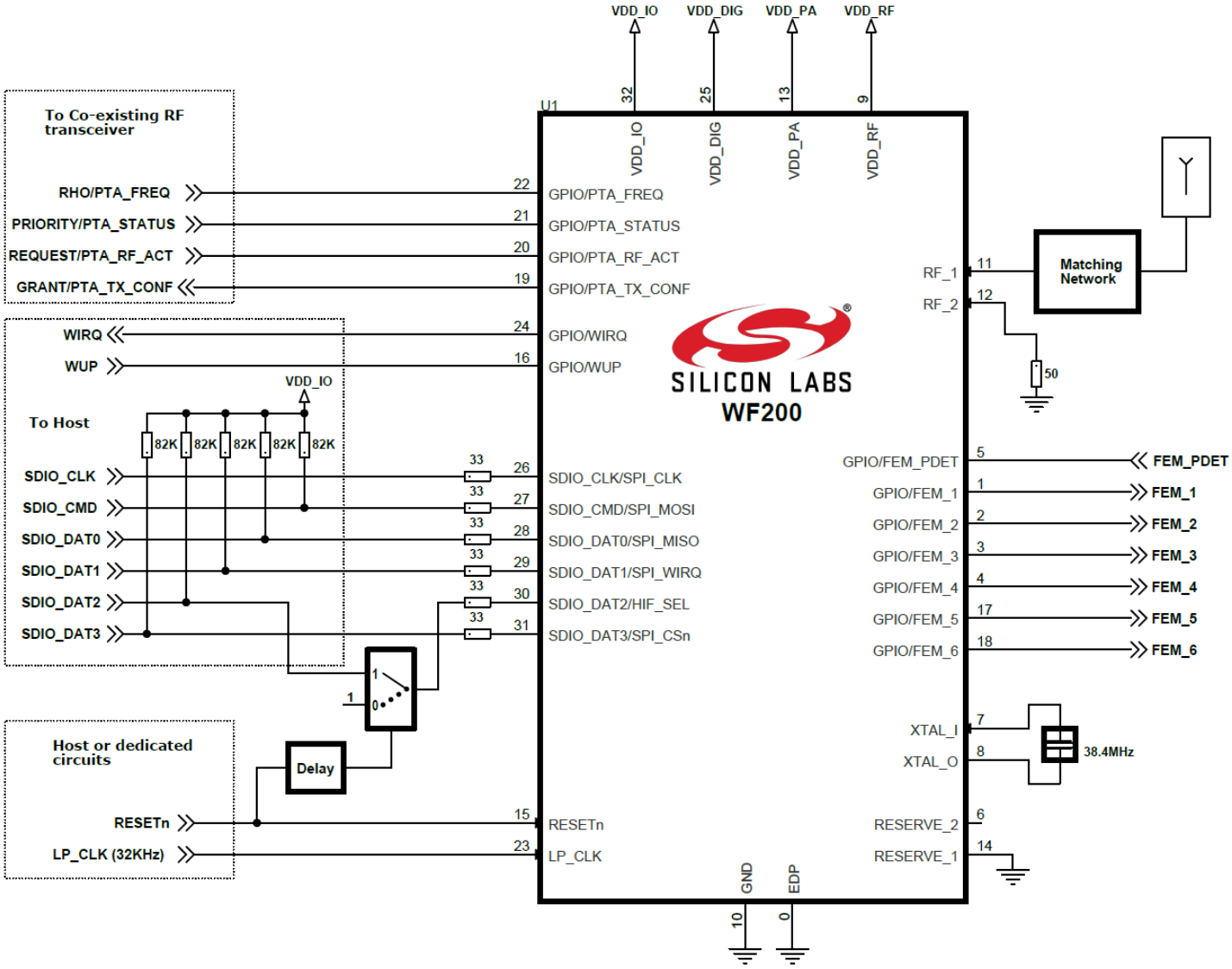


Figure 5.1. Typical Application Circuit SDIO Host Interface

Note:

- The SDIO pin pullup resistors are only required if the Host does not integrate internal pull-ups on SDIO signals as required by the SDIO standard.
- Refer to UG382: WF200 Hardware Design User's Guide for more details on the application circuit.

5.2 Typical Application Circuit for SPI Host Interface

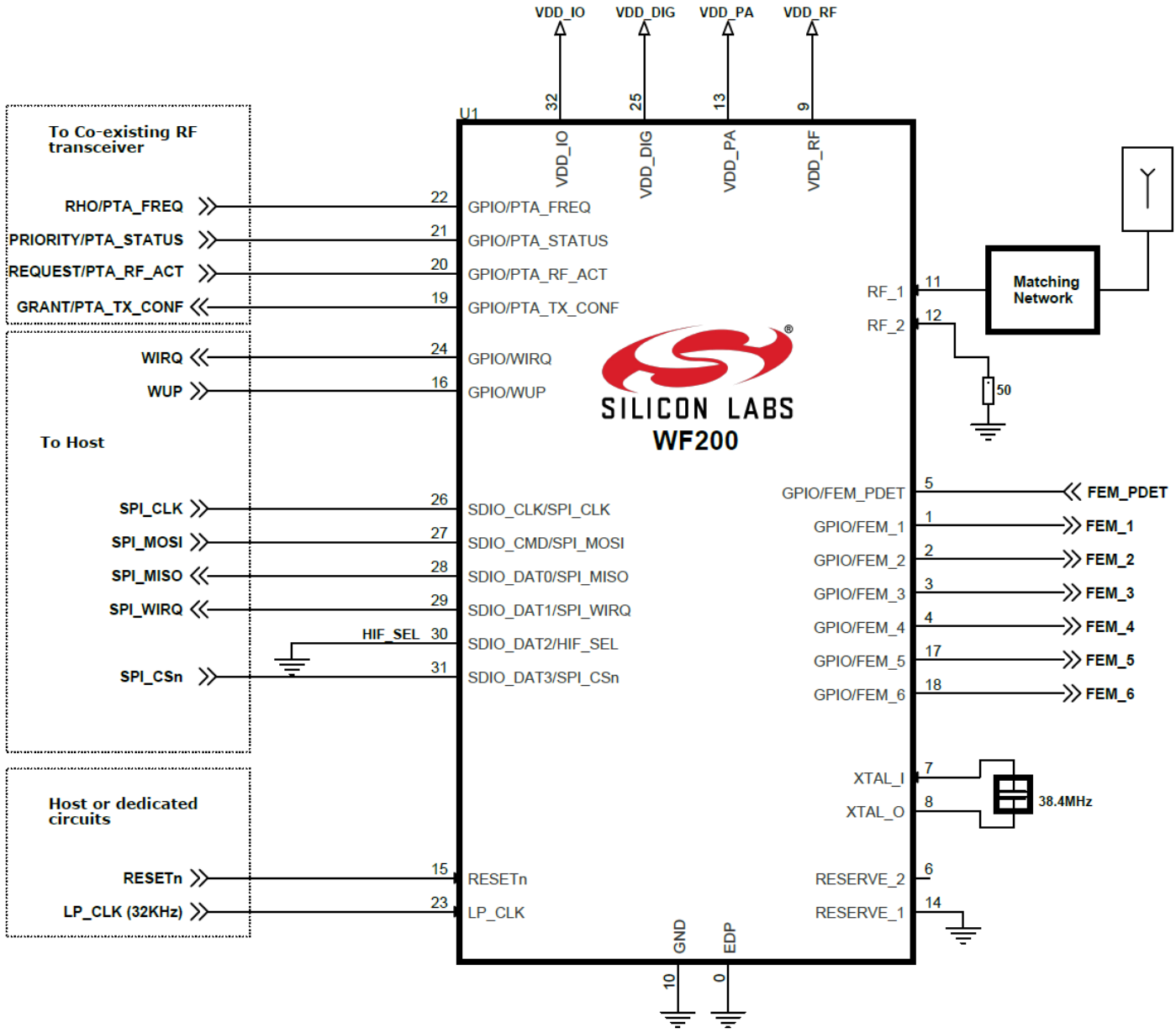


Figure 5.2. Typical Application Circuit SPI Host Interface

Note:

- Refer to UG382: WF200 Hardware Design User's Guide for more details on the application circuit.

5.3 Power States and Low-Power Modes

The current consumption on WF200 is highly dynamic. It varies significantly depending on its activity, the activation of power-save modes, and when it is in shutdown.

There are four main modes, each of them having several power states as detailed below.

Traffic mode: The Traffic mode is defined as the mode when WF200 is transmitting data, receiving data, or listening to the channel. If power save is not activated, the device stays in listen mode when there is no traffic. Current consumption is similar between receive and listen modes, while it is higher during transmission.

Power save modes: When power save mode is activated, the device goes to a low-consumption mode and wakes-up periodically to listen to network beacons, so the device stays associated to the network. The current consumption, while receiving beacons, is as mentioned above for reception.

There are three power-save/low-power consumption cases:

1. Sleep: If a 32 KHz clock is available at LP_CLK input, then the device goes in sleep mode between reception of beacons. In this mode, most of the chip is turned off (including Xtal oscillator and host interface) to reduce the power consumption as much as possible. Given that the host interface is shut down in this mode, the host should assert the WUP pin to wake up the device before any communication with the host can be achieved.
2. Sleep with XO on: If low-power clock is not available on LP_CLK or if the Xtal oscillator cannot be shut down if the Xtal is shared, then the device goes in "Sleep with XO on" mode between reception of beacons. In this mode, the Xtal oscillator is active, so the typical consumption is higher.
3. Snooze: If low-power clock is not available on LP_CLK then the device goes in snooze mode between reception of beacons. In this mode, a smaller part of the device is shut down and the XO is always enabled, so the typical consumption is higher.

The sleep or snooze state/mode can also be achieved when not associated if the firmware decides there are no tasks to perform when the wake-up signal (pin GPIO/WUP) from host is low.

Shutdown mode: Shutdown mode is the case where the transceiver is shut down and reaches the lowest power consumption while still being connected to the power supplies. Getting out of stand-by requires a complete start-up sequence triggered by RESETn pin being set from low to high.

Reset mode: When RESETn is low, the consumption is typically 76 µA, mainly due to the RESETn pull-up resistor within the device.

5.4 RF Connections

5.4.1 Antenna Ports

This device has two RF ports to allow antenna diversity using an internal switch. In applications with only one antenna, the un-used port should be terminated to ground through a resistor between 47 to 51 Ohm. In applications desiring to use a Front End Module (FEM), one of these ports could be used for Transmit, and the other RF Port for Receive.

5.4.2 Antenna Diversity

In Applications where the main antenna is subject to obstruction or de-tuning, a second antenna can be used at the alternate antenna port by using the switched antenna diversity report. The location of this second antenna should be such that both cannot be prevented from operating satisfactorily by the same event. A firmware feature can be invoked to determine which antenna has a better path to the remote WiFi Device.

5.4.3 FEM Support

WF200 supports the use of an external Front End Module (FEM) for customers desiring higher output power than what is provided by the built-in RF front end inside WF200. The device has a low power PA that can be used to drive an external FEM. The following plots can be used to help configure the FEM power levels and settings so that the system has adequate margin to EVM, FCC restricted band emission and mask margin.

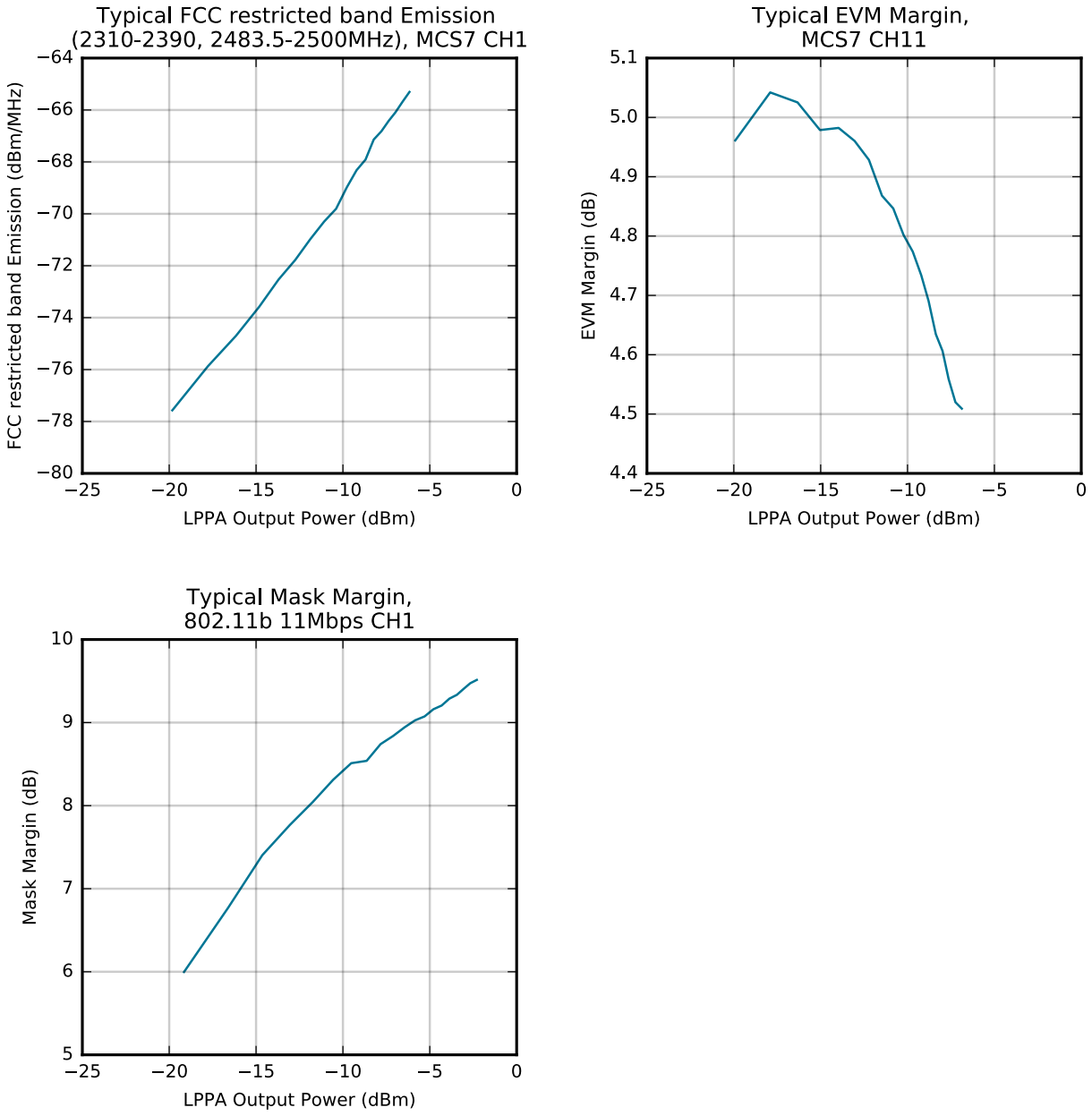


Figure 5.3. Low Power PA Emissions and Margin

5.5 Clocks

5.5.1 XTAL_I and XTAL_O connections for Crystal

Connect the signal pins of a 38.4MHz crystal to the XTAL_O and XTAL_I pins with very short traces. These traces on the PCB should have short length, and minimal parasitic load. There is normally no need for external parallel capacitors because this IC includes internal load capacitors which have programmable values. The value of these load capacitors will have to be determined which center the operating frequency for the design of the crystal and PCB. This value will have to be included in firmware. Firmware will program the prescribe load capacitance prior to startup, and the value should not change during operation. See UG382: WF200 Hardware Design Users Guide for more details of the crystal connections to this IC.

5.5.2 XTAL_I and XTAL_O connections for TCXO

When using a TCXO to provide 38.4MHz clock input, a series 1000pF capacitor is required between the TCXO output pin and XTAL_I pin to block DC. The XTAL_O pin can be left unconnected.

5.5.3 LP_CLK Port

A 32.768KHz clock source should be supplied to LP_CLK pin to enable the lowest power operation in power save modes. The frequency tolerance of this source affects wake up scheduling.

5.6 Multi-Protocol Coexistence

In case an RF transceiver using the same 2.4 GHz band (e.g. Bluetooth, Zigbee, or Thread) is co-located with the WF200 Wi-Fi transceiver, the Packet Traffic Arbitration (PTA) interface can be used to minimize mutual interference. In this case, PTA pins are connected to the other transceiver. The PTA interface is highly programmable and can use 1, 2, 3, or 4 pins upon configuration. WF200 embeds a Packet Traffic Arbitration block in order to share the access to the RF medium between WLAN and another standard.

Depending on manufacturer, PTA signal names can vary and the table below shows some alternative naming:

Table 5.1. PTA Alternative Naming

WF200 Pin Name	Alternative Names
PTA_TX_CONF	GRANT, WL_ACTIVE, WL_DENY
PTA_RF_ACT	REQUEST, BT_ACTIVE
PTA_STATUS	PRIORITY, BT_STATUS
PTA_FREQ	FREQ, BT_FREQ

PTA interface configuration is also achieved via the configuration file.

See https://docs.silabs.com/wifi/wf200/additional-resources#documentation for more information regarding PTA and coexistence management on WF200, as well as AN1017 and AN1128 for EFR32BGx and EFR32MGx devices supporting BLE, Zigbee, and Thread.

6. Pin Descriptions

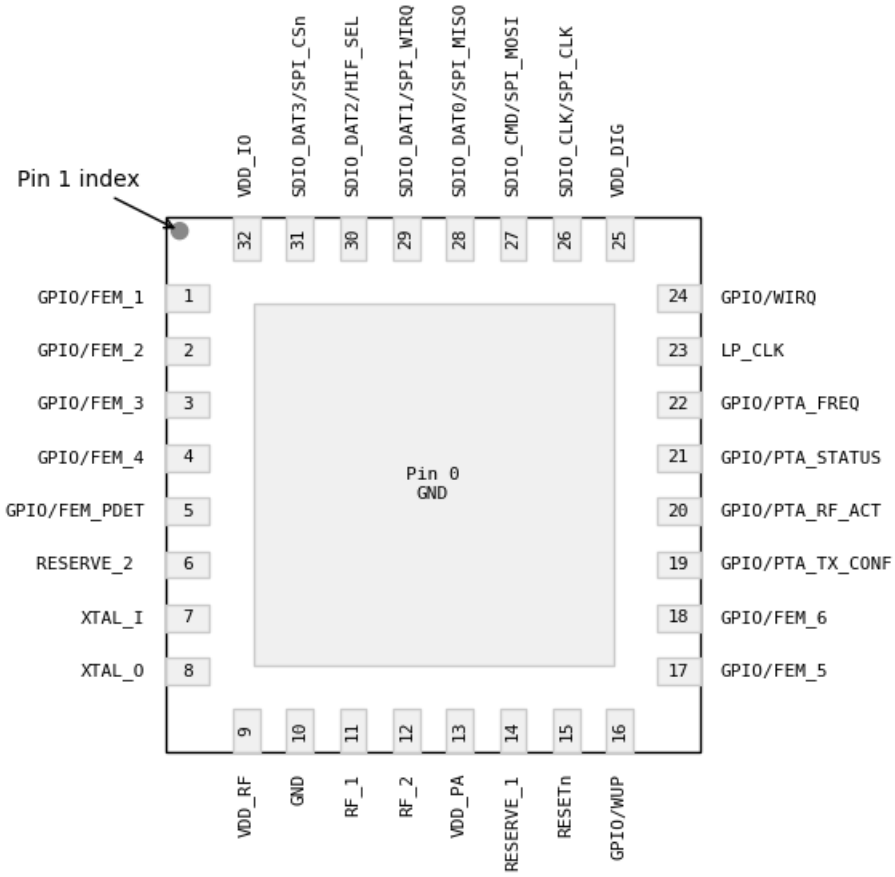


Figure 6.1. WF200 Pinout

Table 6.1. Pin Definitions

Pin #	Pin Name	I/O	Description / Default
1	GPIO/FEM_1	I/O	This pin can be used for dynamic control of an external front-end module (FEM), otherwise this can be used as GPIO.
2	GPIO/FEM_2	I/O	This pin can be used for dynamic control of an external front-end module (FEM), otherwise this can be used as GPIO.
3	GPIO/FEM_3	I/O	This pin can be used for dynamic control of an external front-end module (FEM), otherwise this can be used as GPIO.
4	GPIO/FEM_4	I/O	This pin can be used for dynamic control of an external Power amplifier detector output (Vdet) in case an external power amplifier or a FEM is used. Otherwise this can be used as GPIO.
5	GPIO/FEM_PDET	I/O	Programmable Pins / FEM Power detector Interface
6	RESERVE_2	I/O	Reserved. This pin should be left unconnected.
7	XTAL_I	I	Crystal pin 1 (or reference clock input if driven by TCXO)
8	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I driven by TCXO)
9	VDD_RF	I	RF power supply

Pin #	Pin Name	I/O	Description / Default
10	GND	GND	Ground
11	RF_1	I/O	RF Port 1 to connect to main antenna
12	RF_2	I/O	RF Port 2 to connect to diversity antenna
13	VDD_PA	I	PA Power Supply
14	RESERVE_1	GND	Reserved. For normal operation, this pin must be grounded
15	RESETn	I	Reset pin, active low
16	GPIO/WUP	I/O	This pin can be used to wake up the device from sleep mode, or used as a GPIO
17	GPIO/FEM_5	I/O	This pin can be used to dynamically control an external front-end module (FEM), otherwise this can be used as GPIO.
18	GPIO/FEM_6	I/O	This pin can be used to dynamically control an external front-end module (FEM), otherwise this can be used as GPIO.
19	GPIO/PTA_TX_CONF	I/O	As part of PTA interface, this pin can be used to manage co-existence with another 2.4 GHz radio or can be used as a GPIO
20	GPIO/PTA_RF_ACT	I/O	As part of PTA interface, this pin can be used to manage co-existence with another 2.4 GHz radio or can be used as a GPIO
21	GPIO/PTA_STATUS	I/O	As part of PTA interface, this pin can be used to manage co-existence with another 2.4 GHz radio or can be used as a GPIO
22	GPIO/PTA_FREQ	I/O	As part of PTA interface, this pin can be used to manage co-existence with another 2.4 GHz radio or can be used as a GPIO
23	GPIO/LP_CLK	I	Low Power clock input. This pin is typically connected to the 32 KHz reference clock.
24	GPIO/WIRQ	I/O	In SDIO mode, this pin is an interrupt pin from WF200 to host to indicate a message or data should be read. In SPI mode, this pin can be used as a GPIO.
25	VDD_DIG	I	Digital Power Supply. Identical to VDD_D
26	SDIO_CLK/ SPI_CLK	I	Host interface: SDIO_CLK or SPI_CLK
27	SDIO_CMD/ SPI_MOSI	I/O	Host interface: SDIO_CMD or SPI_MOSI
28	SDIO_DAT0/ SPI_MISO	I/O	Host interface: SDIO_DAT0 or SPI_MISO
29	SDIO_DAT1 / SPI_WIRQ	I/O	Host interface: SDIO_DAT1 or WIRQ
30	SDIO_DAT2/ HIF_SEL	I/O	Host interface selection: Used to select the host interface during reset rising edge. If Low, selects SPI interface. When High, selects SDIO interface and this pin becomes SDIO_DAT2
31	SDIO_DAT3/ SPI_CSn	I/O	Host interface: SDIO_DAT3 or SPI_CSn
32	VDD_IO	I	IO Power Supply
0	GND	GND	Exposed Die Pad

7. Package Outline

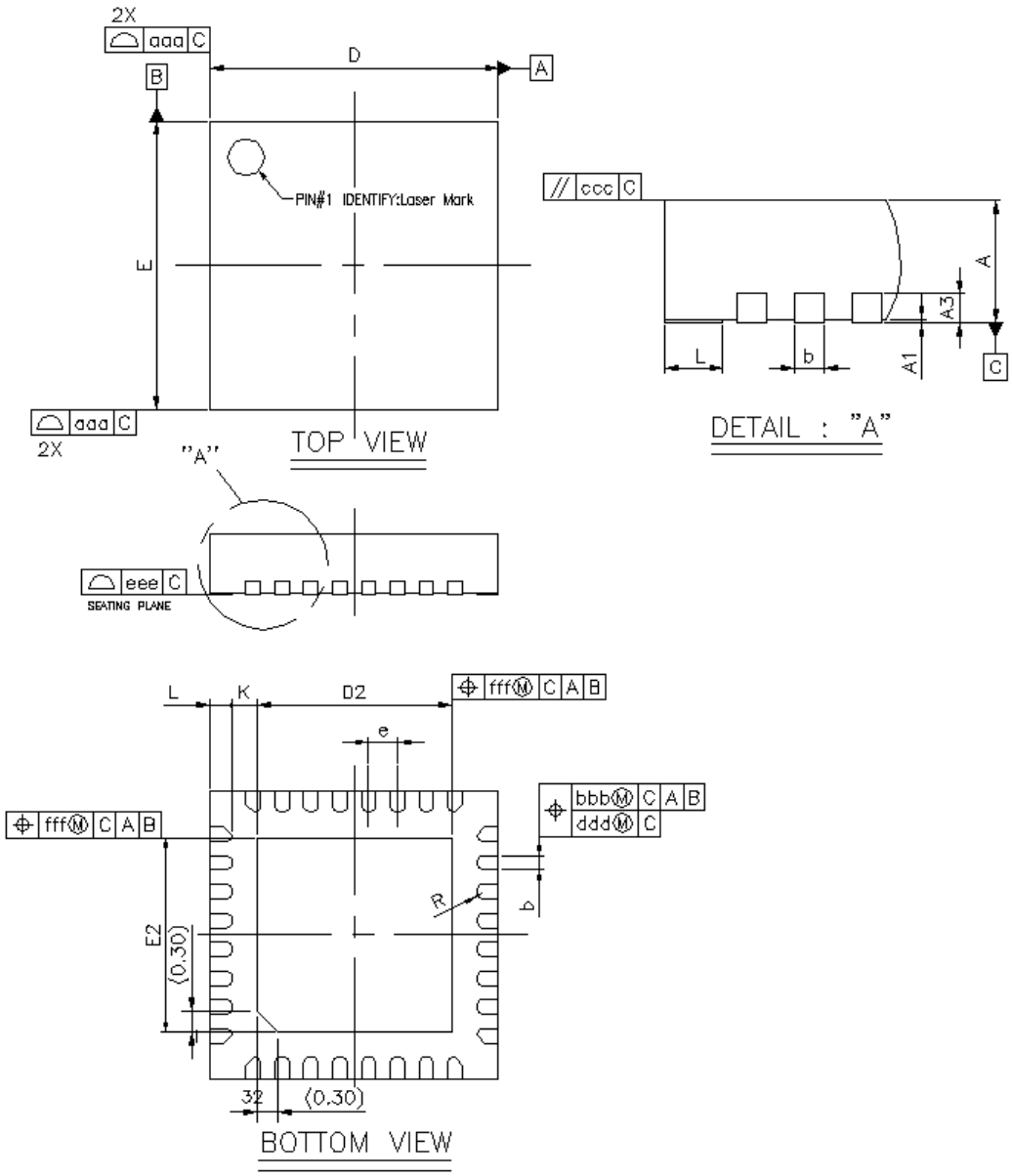


Figure 7.1. WF200 Package Outline

Table 7.1. WF200 Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.40 BSC		
L	0.20	0.30	0.40
K	0.20	---	---
R	0.075	---	0.125
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

8. Land Pattern

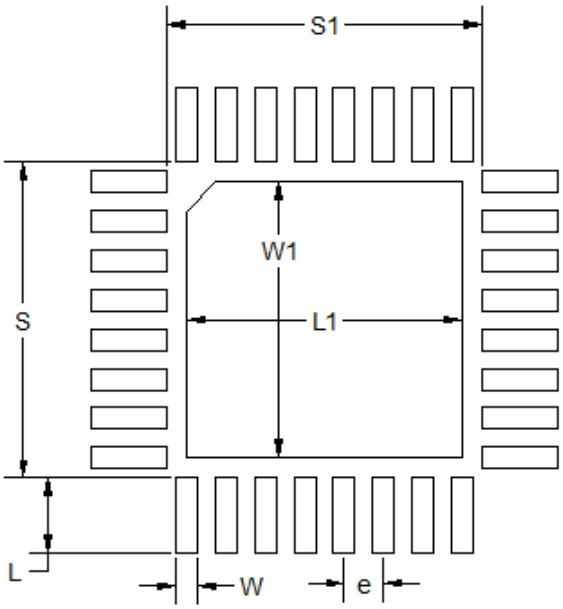


Figure 8.1. WF200 Land Pattern

Dimension	mm
L	0.76
W	0.22
e	0.40
S	3.21
S1	3.21
L1	2.80
W1	2.80

General

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.101mm (4 mils).
- The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
- A 2x2 array of 1.10mm x 1.10mm openings on 1.30mm pitch should be used for the center ground pad.

Card Assembly

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Note: Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

9. Top Marking

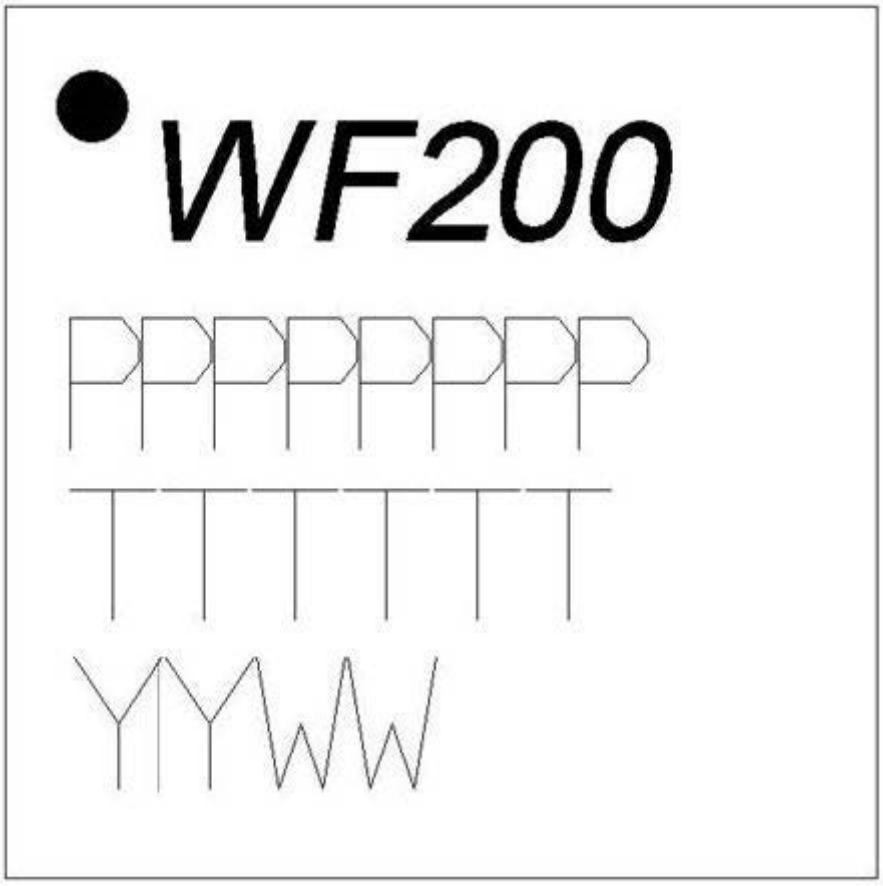


Figure 9.1. WF200 Top Marking

Table 9.1. Top Marking for WF200

OPN	PPPPPPPP	TTTTTT
WF200SD	SD	
WF200D	D	
Note: YY = Year. WW = Work Week		

10. Software Reference

This section gives a short overview of the software involved to run applications based on this device. The firmware running in the WF200 allows it to be used at Lower MAC level (in split MAC) or at the Upper Mac level (in Full MAC).

10.1 Host and Device Software

This device is intended to be used as a Network Co-Processor (NCP) which means that it requires a host processor to run the application. Depending on architecture choices based on required throughput, host memory size and power, the MAC layer can be split between WF200 and its host or fully ran in WF200.

10.1.1 Split MAC

The so-called split MAC is the case where WF200 runs the Lower MAC section while the host processor runs the Upper MAC. This is a use case that typically fits the Linux application as MAC802.11 is provided with Linux

For such an application, Silicon Labs provides the embedded firmware implementing the Lower MAC as well as needed configuration tasks. Sample core Linux drivers are available for a variety of platforms.

The figure below shows the typical software architecture in Split MAC implementations.

Figure 10.1. Split MAC Implementation

10.1.2 Full MAC

In this scenario, both the lower MAC and upper MAC are running in WF200. The WF200 contains a WPA/WPA2 personal supplicant, allowing it to handle full MAC responsibilities without utilizing the host MCU. The host receives an IP packet and implements all stack layers necessary above it.

The figure below shows the typical software architecture in Full MAC implementations.

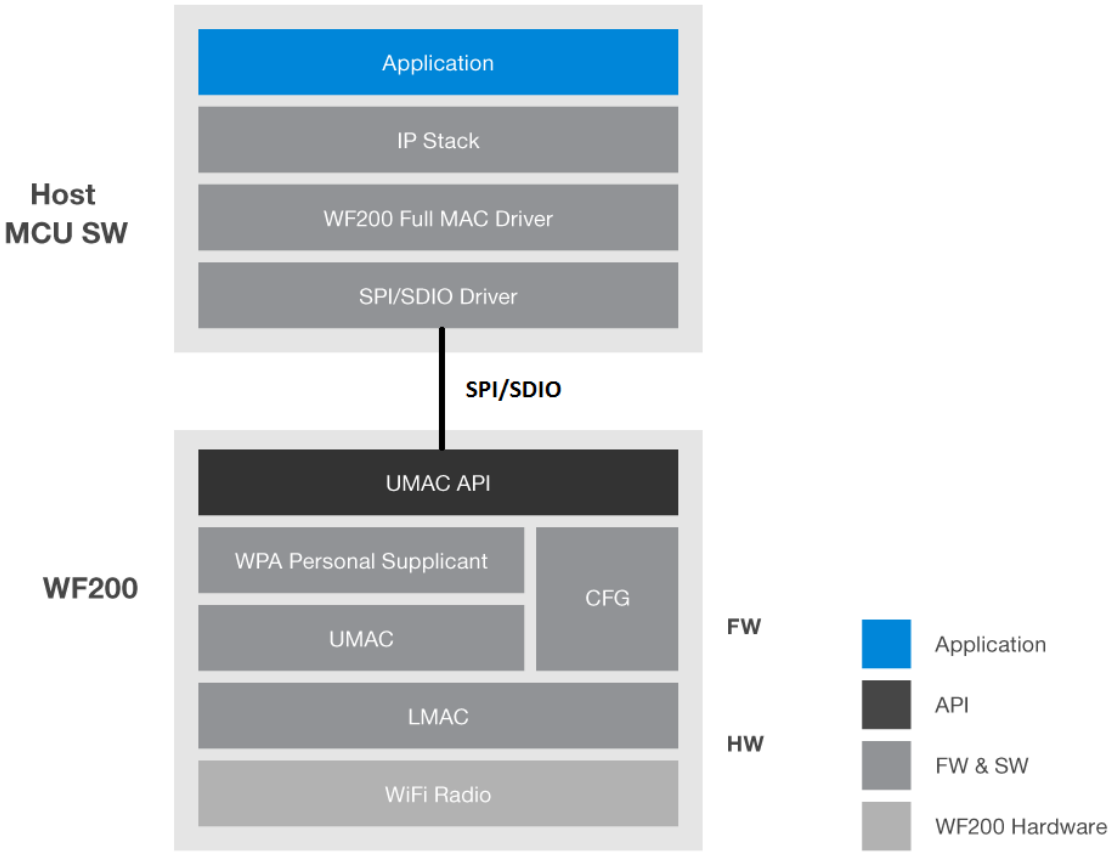


Figure 10.2. Full MAC Implementation

Note: The WPA supplicant on WF200 does not support WPA enterprise. If WPA-enterprise is required, then it should be implemented above the IP stack in the host MCU software.

10.1.3 Software Documentation

Documentation required for software implementation is available at https://docs.silabs.com/.

10.2 Security

The WF200 implements several security features as listed below.

10.2.1 Secure Device

WF200 disables access to all debug ports.

10.2.2 Secure Boot

Secure Boot includes several features related to boot and firmware security. Firmware authentication and encryption do not have any impact on host software, whereas firmware roll back prevention requires more flexibility and is managed by each customer through software.

- Firmware authentication: The downloaded firmware is authenticated such that only Firmware provided by Silicon Labs can run in WF200.
- Firmware encryption: The downloaded firmware is encrypted when generated by Silicon Labs and is decrypted inside WF200 during firmware download.
- Firmware roll back prevention: If a security threat is discovered, Silicon Labs has the ability to increment in its firmware an anti-roll-back tag. This can be used by the customer to prevent the part from starting with a firmware having a tag lower than a specified one. This mechanism is managed by each customer on a case-by-case need.

10.2.3 Secure Link (WF200SD only)

Secure Link refers to the capability to have encrypted SPI/SDIO communication between the host and WF200. This feature requires the host and WF200 to exchange a key based on a shared secret stored on both sides nonvolatile secured memories and programmed at the end product manufacturing stage. The encrypted interface uses a Diffie-Hellman algorithm key exchanges on a per session/per device basis. As a result, a given link is secured uniquely on a given device, and keys are regenerated on a power cycle.

There are 3 possible cases for secure link:

- Secure link is not used: In this scenario, the part does not encrypt any communication with the host.
- Secure link is temporary enabled: Secure Link can be activated through software, with a software key which is not stored in WF200. Doing this allows to assess the performance and consumption impacts of secure link. In this mode, Secure Link is achieved as long as the part is not reset. The next restart of WF200 will make it start in Non-Secure Link mode.
- Permanent Secure Link: This mode is activated by software and the key exchanged is permanently stored in WF200 non-volatile memory. Once configured in this mode, WF200 only understands host interface messages which have been encrypted with the stored key.

Once a secure link has been established, the host can choose to only encrypt certain API messages between the host and the WF200 to reduce the power and latency overhead of encryption.

10.3 Startup, Sleep and Shutdown

10.3.1 Power On, Reset, and Boot

When RESETn pin is set HIGH, WF200 is getting out of its reset mode. All supply voltages should be settled within the operational range before the rising edge of RESETn pin. Then the boot sequence can be initiated by the host software with the following sequence:

- Some registers describing the required configuration before firmware download are written by the driver.
- The driver initiates the boot.
- The driver downloads the embedded firmware into WF200.
- The driver configures WF200 upon the hardware platform and requested features with a dedicated configuration file.

10.3.2 Sleep and Snooze Modes

The sleep or snooze modes are reached when power-save mode has been enabled on the WF200. These modes highly reduce power consumption while maintaining all configuration and context, so that the device can be quickly back to normal operation. A WF200 driver command is used to indicate that the driver wants the part to go to power-save. However it is the firmware on WF200 that decides when it switches into sleep mode based on Wi-Fi activity.

The part wake-up is achieved by asserting the GPIO/WUP pin.

The sleep mode requires a 32 KHz clock to be provided on LP_CLK pin.

In case a 32 KHz clock is not available, the part can be set in a snooze mode which is functionally equivalent but draws more current.

10.3.3 Shutdown Mode

The shutdown mode can be used if the Wi-Fi feature is not needed for a long period of time. This mode achieves the lowest current consumption on the device but requires a full power-up reset and boot sequence to come back to the operational mode. This mode should be initiated by the host.

Note: A similar behavior could be achieved by asserting RESETn pin low, but would draw more current.

11. Revision History

Revision 1.1

September, 2020

- Updated Ordering Guide
- Updated Table 9.1 Top Marking for WF200 on page 32

Revision 1.00

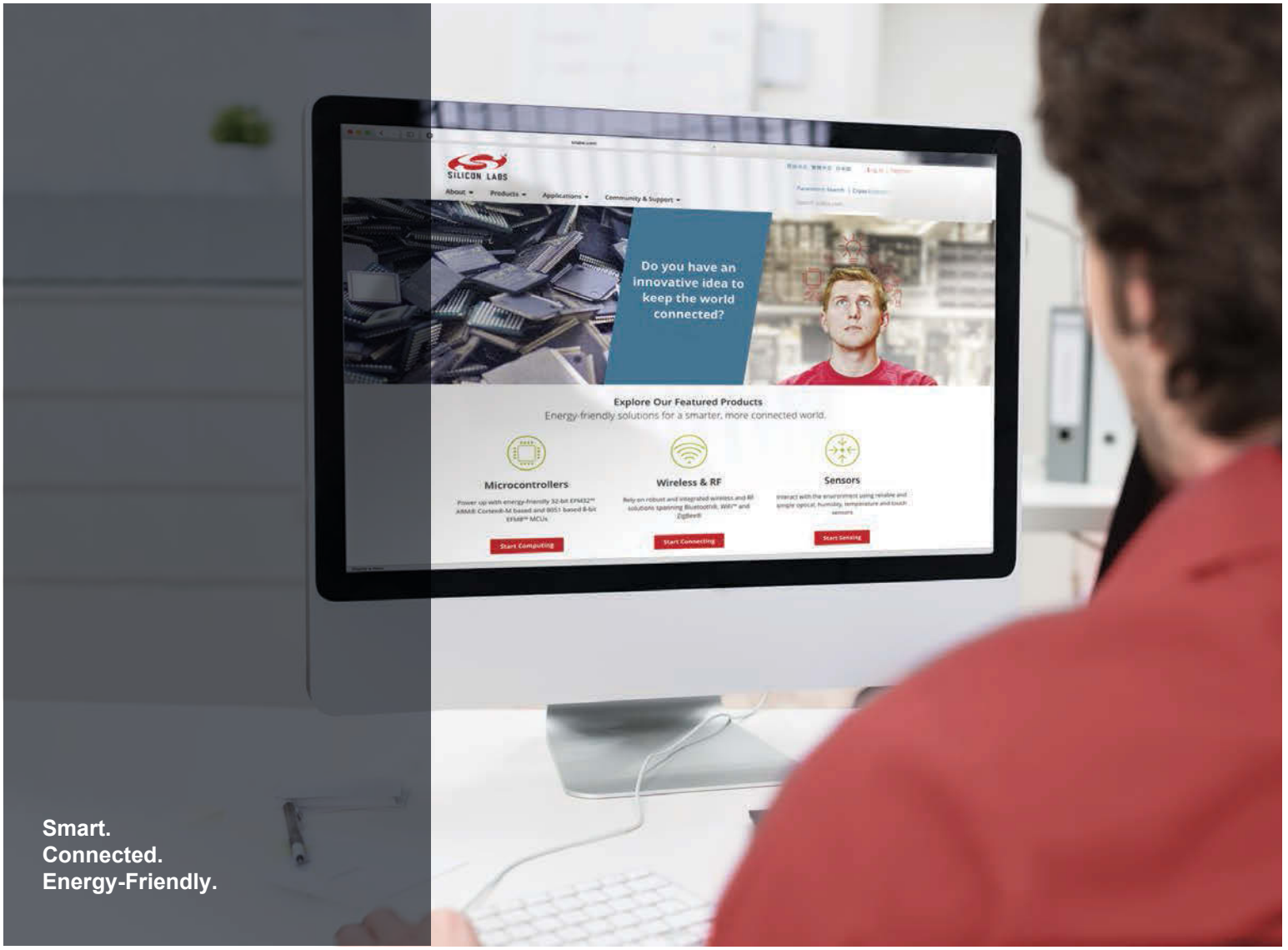
July, 2019

- Updates to Electrical specifications section
- Addition of low power PA graphs
- Updates to power consumption and supported bandwidth and channels table
- Textual and figure updates to improve clarity

Revision 0.60

December, 2018

- Initial Release



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